REMARKS

Claims 6-9 and 11-19 are pending in the present application. Claims 6, 11, 14 and 16 have been amended.

Claim Rejection-35 U.S.C. 102

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Yoo et al. reference (U.S. Patent No. 5,605,853). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 16 includes in combination first and second gates; a field oxide; side walls; a protective layer "formed selectively on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by side walls"; and an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate. Applicant respectfully submits that the Yoo et al. reference as relied upon by the Examiner does not disclose these features.

In the Final Office Action dated January 10, 2003, the Examiner has interpreted floating gate 21 as illustrated in Fig. 7 of the Yoo et al. reference as the protective layer of claim 6. However, as may be readily understood in view of Fig. 7 of the Yoo et al. reference, sidewall spacers 20 are formed adjacent on floating gate 21. The Yoo et al. reference therefore does not disclose a protective layer having edges that are not covered by side walls. An improved alignment margin for contact holes to a protective

layer and high quality connections as in the present invention are thus not provided in the Yoo et al. reference. Applicant therefore respectfully submits that the semiconductor device of claim 6 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection of claims 6-9 is improper for at least these reasons.

The semiconductor device of claim 11 includes in combination a gate; a field oxide; a protective layer "formed on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by side walls"; and an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate, whereby the protective layer is formed only on the field oxide.

As emphasized previously, the edges of floating gate 21 in Fig. 7 of the Yoo et al. reference are covered by sidewall spacers 20, and thus cannot be interpreted as the protective layer of claim 11. Applicant therefore respectfully submits that the semiconductor device of claim 11 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection of claims 11-15 is improper for at least these reasons.

The semiconductor device of claim 16 includes in combination a gate; side walls; a field oxide; a protective layer "formed on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by

side walls"; and an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate, the protective layer being formed only on the field oxide.

Applicant respectfully submits that the Yoo et al. reference does not disclose a protective layer as featured in claim 16. Accordingly, Applicant respectfully submits that the semiconductor device of claim 16 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection of claims 16-19 is improper for at least these reasons.

Conclusion

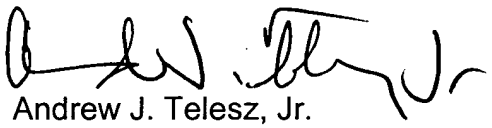
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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